Peripheral Component Interface (PCI)

Background

In its simplest terms, the computer bus moves data between the CPU, memory, and peripherals. One of the first buses, the Personal Computer (PC) bus, was built by IBM in 1981. It was based on 8-bit architecture meaning that with each cycle, 8 bits (1 byte) could travel through the bus.

In 1984, IBM developed the Advanced Technology (AT) bus. The AT bus could transmit data at 16 bits per cycle and was such a success it became known as the Industry Standard Architecture (ISA) bus. Vendors began to clone the IBM PC and used the ISA bus to deliver transfer speeds of up to 5MB/sec in their systems.

In 1987, IBM introduced a new bus called Micro-Channel Architecture (MCA). This bus was a 32-bit bus that was faster and more reliable. IBM intentionally created the bus to be non-compatible with the ISA architecture. If customers wanted Micro-Channel Architecture they had to bypass the clone makers and buy directly from IBM. All peripheral cards used previously in ISA machines could not be used in the MCA machines.

As a counter to IBM's new, higher performing MCA bus, nine companies formed an alliance to develop and standardized a new open bus architecture. They went by the acronym WATCHZONE, with each company's initials being used in the acronym. The companies were Wyse, AST, Tandy, Compaq, Hewlett-Packard, Zenith, Olivetti, NEC, and Epson. They built a 32-bit bus which was backward compatible with ISA and called the bus EISA, or Extended Industry Standard Architecture.

Another short lived effort to increase bus bandwidth and speed was the 32 bit VESA Local bus (VL Bus). The VL Bus and was designed as a peripheral bus that was primarily used in 486 PCs. It allowed high-performance peripherals to bypass the I/O bottlenecks of traditional system buses, thereby taking a shortcut to the system processor. While VESA was a good short-term solution, it has a number of limitations. Those limitations include:

- The VL bus is tied to the processor’s speeds so not every VL bus card is compatible with every VL bus based system.
- The peripherals that work with the VL system must run at the same speed as the processor. A 50 MHz processor would need a peripheral that ran at 50 MHz and this would make the peripheral extremely rare and expensive.
- Because the VL bus is an extension of the local CPU bus it is limited in I/O slots.
- The VL bus is only a 32 bit bus and cannot be expanded to 64 bits. It is really only applicable with 486 chips.

Neither MCA, EISA, nor VESA bus technology could keep pace with the rapid development and speed of the CPU chip, and in 1991 Intel Corporation began working on the Peripheral Component Interface (PCI) bus, which would increase the bandwidth and reduce the cost of bus architecture.

PCI

The PCI (Peripheral Component Interconnect) bus began as a local bus. A local bus takes peripherals off the I/O bus and connects them, together with the CPU and the memory subsystem, to a wider, faster pathway for data. In simple terms, a local bus allows different peripherals to read from, or write to, main memory quickly. PCI began as an advanced high-performance local bus that supports multiple peripherals and has since grown into an I/O bus and an expansion bus.

The PCI local bus was jointly developed by Intel and other industry leaders in order to bring current and next-generation PCs to new levels of systems performance. The objectives for PCI were:

- High performance - greater than 100 MB sustainable
- Low cost
- Longevity
- Software compatibility

- Add-in cards compatible with any system

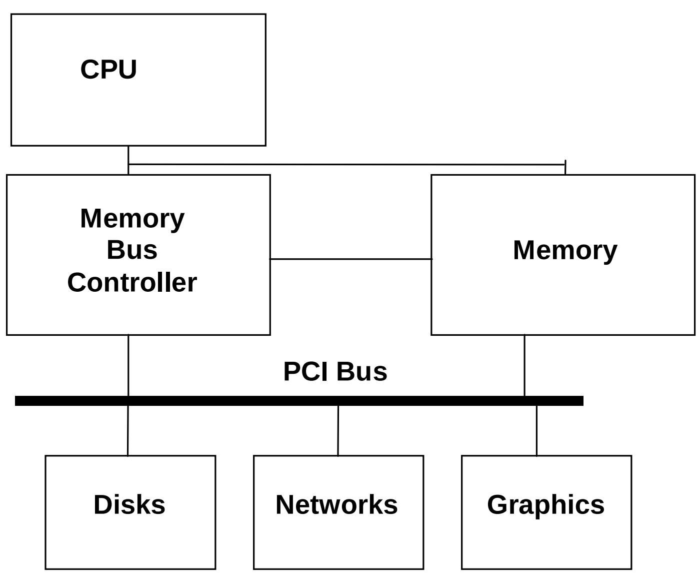
PCI takes advantage of today's microprocessor and personal computer technology and provides a total system solution. A major feature of PCI is that it is compatible with existing ISA, EISA and Micro Channel expansion buses.

Peripherals supported by PCI include;

- Network adapters
- Hard disk drives
- Full motion video
- Graphic accelerators
- Audio cards

The picture below shows the PCI connecting peripherals which read or write to main memory quickly. The local bus was originally designed for graphics, but has since grown to include LAN, disk drive interfaces and SCSI cards.

PCI as a local bus



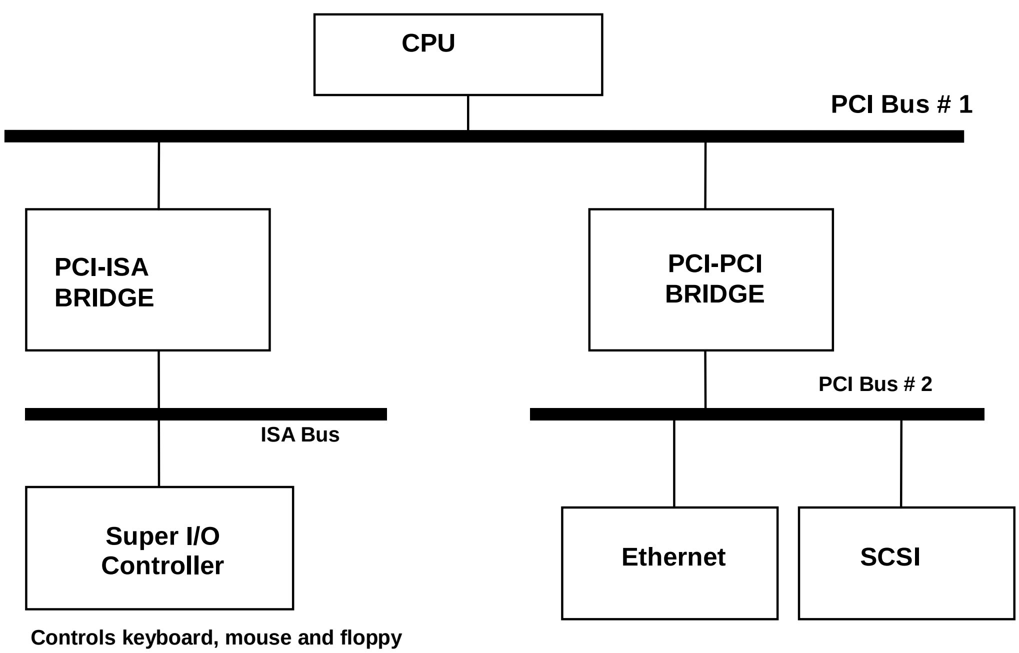
How does PCI work?

PCI occupies an intermediate level between the CPU local bus (processor/memory/cache subsystems) and a standard expansion bus (ISA, EISA, Micro Channel). The PCI bus is isolated from the CPU local bus by a PCI bridge/controller. The CPU can write data to peripherals such as a hard drive and the PCI bridge/controller can immediately store the data in its buffer. This lets the CPU go on to its next operation rather than waiting for the transfer to complete. The buffer then feeds the data to the peripheral at the most efficient rate possible.

PCI also supports bus masters. Bus masters are intelligent devices, which when attached to a system bus, can gain control of the bus and perform tasks independent of the CPU.

The picture below shows an example of a PCI based system. The PCI buses and PCI-PCI bridges are the glue connecting the system components. A PCI-PCI bridge connects the primary bus to the secondary PCI bus. The CPU is connected to PCI bus 1. The PCI-ISA bridge in the system supports older, legacy ISA devices. The diagram also shows a super I/O controller chip which controls the keyboard, mouse and floppy.

PCI Used With Older Legacy Buses



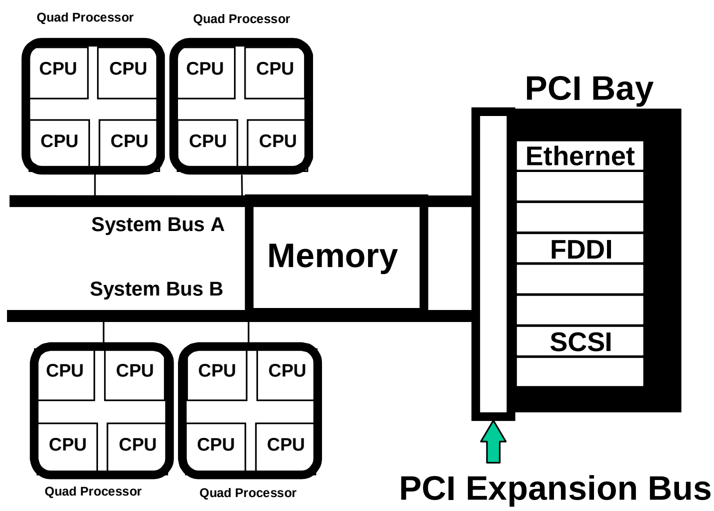
PCI as an Expansion Bus

The PCI bus has grown from its original use as a local bus to industry-wide use as an I/O expansion bus. An expansion bus works with the I/O bus and allows for system expansion. The PCI bus runs at 132 MB/second, which is four times the EISA bandwidth.

The PCI bus incorporates many advanced features that enable intelligent I/O subsystems to contribute to increased system performance and superior load balancing between applications and I/O processing. Many manufacturers of larger servers use the PCI bus for high-performance open server platforms.

The picture below shows a multiprocessor system utilizing PCI as an expansion bus. LAN, disk drive controllers, and SCSI cards utilize a bay to connect the peripheral to the CPUs and memory.

PCI Used as an Expansion Bus



Comparison of different bus architectures

There are many key items you must consider when comparing bus standards. The speed of the bus is important. It affects how quickly data can be transferred. Another factor is the number of slots. The number of slots directly limits the number of peripherals that can be added to the system.

Future upgrades of the CPU can also be affected by bus architecture. If the system can be upgraded it will have a longer life span. PCI is built for CPU upgrades. It can handle faster CPU's because it runs at 33MHz. Since PCI is a 32-bit bus which can generate a heartbeat of 33 million events per second, we see transfer rates of 132 MB/sec. PCI can also be expanded to a 64-bit architecture having a bandwidth of 264 MB/Sec. Because the bus sends 32 or 64-bits every cycle or heartbeat, we multiply 32 or 64 times 33 million. This produces tremendous bus speeds of 132 or 264MB/sec.

The chart below is a comparison of the PCI bus and older legacy buses.

BUS Comparison Chart

	ISA	EISA	MicroChannel	VESA	PCI
Data Path Width	8/16	32.00	16/32/64	32	32/64
Data Bus Speed (MHz)	5.33/8.33	8.33	10.00	33/50	33.00
Data Transfer Rate (MB/sec)	5.33/8.33	33.00	20/40/80/160	132	132/264
Data Rates (MB/sec)	5.33/8.33	33.00	80 (RS/6000)	132.00	132.00
Number of Slots	0-8	0-8	0-8	0-2	0-4
Bus Master Supported	NO	YES	YES	YES	YES
Data/Address Parity	NO	NO	YES	NO	YES
Syn, Channel Checks	NO	NO	YES	NO	YES
Card ID/Auto Config	NO	YES	YES	YES	YES
Works with MC/ISA/EISA	N/A	N/A	N/A	YES	YES

PCI Conclusion

The buses of yesterday (ISA, EISA, MCA) were specified for the 286, 386, and 486 computers. These speeds do not provide the performance needed in today's environments. The solution is a local bus or newer expansion bus capable of moving data much more quickly. This bus is the Peripheral Component Interconnect. This intelligent bus takes peripherals off the slower systems bus and connects them, (together with the CPU and the memory subsystem), to a wider, faster pathway for data. The result is faster data transfer between the CPU and the peripherals. Most PCI systems will support multiple performance-critical peripherals. These peripherals are integrated directly onto the motherboard or can be added via PCI expansion cards, such as disk drives, LAN cards, multimedia, and graphics. ISA, EISA or MCA add-in cards can be used because PCI is designed to supplement, not replace, the traditional I/O bus.

Key points to remember:

- ISA, EISA, and MCA are precursors of PCI.
- The Peripheral Component Interconnect (PCI) was designed by Intel and other industry leaders to keep pace with today's microprocessors.
- A local bus can be thought of as a way for different peripherals in a computer to read from or write to main memory quickly.
- PCI began as a local bus. PCI has developed into a local, I/O or expansion bus that is backward compatible to ISA, EISA, and MCA.
- PCI connects LAN's, disk controllers, and SCSI peripherals to a computer.
- PCI is a 32-bit architecture and runs at 33 MHz. This provides a bandwidth of 132 MB/second.
- PCI is capable of expanding to a 64-bit architecture to run with the next generation of processor. This will provide a bandwidth of 264 MB/second.